AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for re-targeting a design, said method comprising the steps of:

receiving a first low-level design representation targeting a first integrated circuit;

transforming said first low-level design representation into a synthesizable, editable, and simulatable high-level design representation; [[and]]

processing said high-level design representation to generate a second low-level design representation targeting a second integrated circuit[[.]]; and

wherein said low-level design representation includes Boolean equations and no IF statement, and said high-level representation is a hardware description language (HDL) that has an IF statement.

2. (Original) The method of claim 1 wherein one of said first and said second integrated circuits is complex programmable logic device.

3. (Original) The method of claim 1 wherein one of said first and said second integrated circuits is field programmable gate array.

4. (Original) The method of claim 1 wherein one of said first and said second integrated circuits is gate array.

5. (Original) The method of claim 1 wherein one of said first and said second integrated circuits is ASIC.

6. (Original) The method of claim 1 wherein said high-level design representation comprises VHDL code.

Claim 7. (Cancelled)

8. (Original) The method of claim 1 wherein said high-level design representation comprises Verilog code.

Claim 9. (Cancelled)

10. (Original) The method of claim 1 wherein said transforming steps comprises the steps of:

parsing said first low-level design representation;

identifying equations in said first low-level design representation that give rise to synthesizable and simulatable objects; and

writing said high-level design representation that contains said synthesizable and simulatable objects.

11. (Original) The method of claim 10 wherein said objects include flip flops.

12. (Original) The method of claim 10 wherein said objects include input, output and inout.

13. (Original) The method of claim 10 wherein said objects include tristate and open drain outputs.

14. (Original) The method of claim 10 wherein one of said first and said second integrated circuits is complex programmable logic device.

15. (Original) The method of claim 10 wherein one of said first and said second integrated circuits is field programmable gate array.

16. (Original) The method of claim 10 wherein one of said first and said second integrated circuits is gate array.

17. (Original) The method of claim 10 wherein one of said first and said second integrated circuits is ASIC.

18. (Original) The method of claim 10 wherein said high-level design representation comprises VHDL code.

Claim 19. (Cancelled)

20. (Original) The method of claim 10 wherein said high-level design representation comprises Verilog code.

Claim 21. (Cancelled)

22. (Currently Amended) A method for re-targeting an electronic circuit design, comprising:

inputting a first low-level, placed-and-routed design specification targeted to a first type of integrated

generating from the first design specification, a high-level, synthesizable, and simulatable design specification; [[and]]

generating from the high-level design specification a second low-level, placed-and-routed design specification targeted to a second type of integrated circuit, wherein the second type differs from the first type[[.]]; and

wherein said low-level design specification includes Boolean equations and no IF statement, and said high-level design specification is a hardware description language (HDL) that has an IF statement.

23. (Previously presented) The method of claim 22, wherein the second type of integrated circuit is a complex programmable logic device.

24. (Previously presented) The method of claim 22, wherein the second type of integrated circuit is a field programmable gate array.

25. (Previously presented) The method of claim 22, wherein the first type of integrated circuit is an ASIC.

26. (Previously presented) The method of claim 22, wherein the high-level design specification includes hardware description language code.

Claim 27. (Cancelled)

28. (Currenlty amended) The method of claim 22 [[27]], wherein the second low-level design specification includes Boolean equations without IF statements.

29. (Currently amended) The method of claim 22 [[27]], wherein generating the high-level specification comprises:

identifying equations in the first low-level design specification having information for synthesizable and simulatable objects; and

writing to the high-level design specification, synthesizable and simulatable objects using the information from the identified equations.

30. (Currently amended) An apparatus for re-targeting an electronic circuit design, comprising:

means for inputting a first low-level, placed-and-routed design specification targeted to a first type of integrated

means for generating from the first design specification, a high-level, synthesizable, and simulatable design specification; [[and]]

means for generating from the high-level design specification a second low-level, placed-and-routed design specification targeted to a second type of integrated circuit, wherein the second type differs from the first type[[.]]; and

wherein said low-level design specification includes Boolean equations and no IF statement, and said high-level design specification is a hardware description language (HDL) that has an IF statement.